Enhancement-Mode Power Heterojunction FET utilizing Re-grown P$^+$-GaAs Gate with Negligible Off-state Leakage Current

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Abstract — **Enhancement-mode power heterojunction FET utilizing re-grown p$^+$-GaAs gate (p$^+$-gate HJFET) was developed for cellular applications. The p$^+$-gate HJFET exhibited a high maximum drain current of 400mA/mm and a gate forward turn-on voltage of 1.15V with threshold voltage (V_T) of +0.5V. A small V_T standard deviation of 20mV was obtained. The 32mm gate width device has an extremely low off-state leakage current of 0.02μA at drain-to-source voltage (V_{ds}) of 3.0V and gate-to-source voltage of 0.0V and at RT. Under single 3.2V operation, the 32mm device delivered 35dBm output power, 11.9dB associated gain and 73% power added efficiency at 950MHz. Even operated at V_{ds} of 1.0V, the device exhibited a high PAE of 70%. The developed p$^+$-gate HJFET is promising for no drain bias switch and single voltage operation power amplifiers.**

I. Introduction

For cellular applications, power amplifier is required to operate with a single voltage supply. Enhancement-mode FET is a good candidate to meet the demand. For the FET, the negligible off-state drain leakage current(I_{leak}) at a gate-to-source voltage (V_{gs}) of 0V is desirable, because the drain bias switch can be eliminated, thus realizing low cost and small size cellular phones. In order to realize the negligible I_{leak}, the high positive threshold voltage (V_T) is necessary. With an increase in V_T close to forward gate turn-on voltage (V_F), however, the forward gate voltage swing was reduced. This degrades DC characteristics, such as a decrease in maximum drain current, and RF power performance of the enhancement-mode FET, therefore increasing V_F becomes the key issue [1]-[4].

In this paper, we demonstrate high power performance enhancement-mode heterojunction FET utilizing re-grown p$^+$-GaAs gate (p$^+$-gate HJFET) with negligible off-state drain leakage current.

II. Device Structure and Fabrication

Fig. 1 shows the cross section view of the developed p$^+$-gate HJFET. In order to increase V_F, pn junction was introduced to double-doped AlGaAs/InGaAs/AlGaAs HJFET. A highly C-doped p$^+$-GaAs layer was formed beneath the gate electrode by selective regrowth metalorganic chemical vapor deposition (MOCVD). The effective gate potential barrier height of p$^+$-gate HJFET is about 1.5eV, which is 0.5eV higher than that of gate metal/AlGaAs Schottky. The p-type dopant C has a low diffusion coefficient, unlike Zn [2], which is favorable to suppress degradation of V_T uniformity during the device fabrication process. A recessed structure was fabricated by high selective electron cyclotron resonance (ECR) plasma dry-etching [5]. The gate length was 0.5μm.

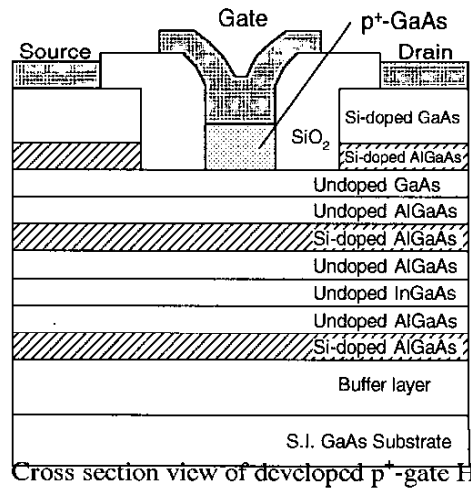

Fig. 1. Cross section view of developed p$^+$-gate HJFET

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III. DC CHARACTERISTICS

Fig. 2 shows forward gate I-V characteristics for p^+-gate HJFET and normal Schottky gate HJFET [6]. The fabricated p^+-gate HJFET achieved a high V_F of 1.15V, which is 0.45V higher than that of the Schottky gate HJFET.

Fig. 3 shows drain I-V characteristics of the p^+-gate HJFET. The device exhibited a maximum drain current (I_{max}) of 400mA/mm and on-resistance (R_{on}) of 1.8 Ω·mm, defined at V_{gs} of +1.2V. The high I_{max} and low R_{on} characteristics are favorable for designing high efficiency small-sized enhancement-mode power FET.

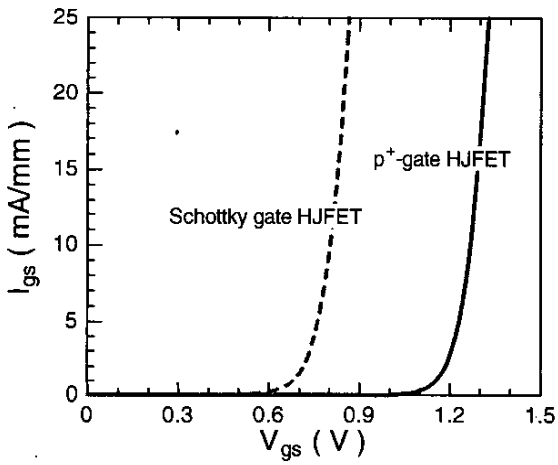

Fig. 2. Forward gate I-V characteristics

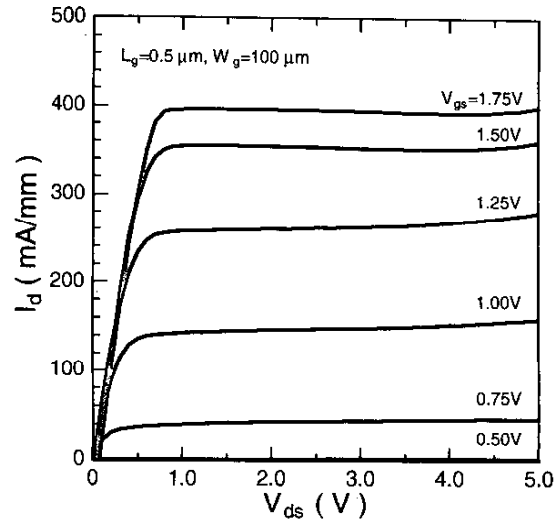

Fig 3 Drain I-V characteristics

Fig. 4 shows the transconductance (g_m) and the drain current (I_d) as a function of V_{gs}. The maximum g_m was 480mS/mm. The V_T, defined at I_d of 1mA/mm, was +0.5V. The gate breakdown voltage, defined at gate-to-drain current of –1mA/mm, was obtained to be 23V, which is sufficiently high for 3V operation.

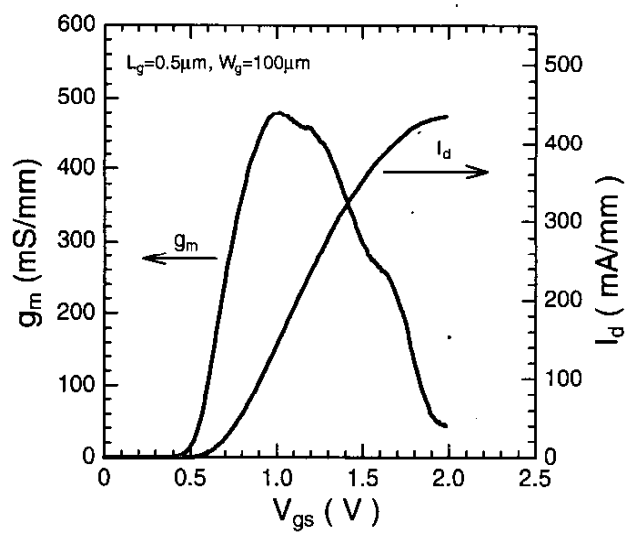

Fig. 4. V_{gs}-g_m, I_d characteristics

Fig. 5 shows V_T uniformity across wafer for p^+-gate HJFET and Schottky gate HJFET. The p^+-gate HJFET demonstrated small standard deviation of about 20mV, which is the almost same as that of the Schottky gate HJFET. This is

because we applied the high selective ECR plasma dry-etching for recess formation and the optimum C-doped p^+-GaAs regrowth condition.

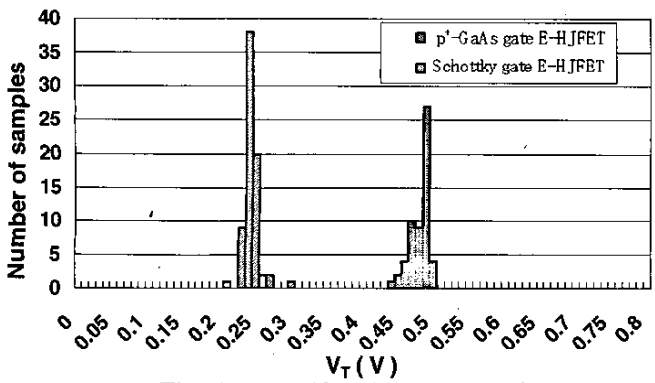

Fig. 5. V_T uniformity across wafer

IV. Leakage Current Characteristics

V_{ds} and the temperature dependence of I_{leak} was evaluated using a 32mm gate width (W_g) p^+-gate HJFET. Fig. 6 shows I_{leak} at 85℃ and RT as a function of V_{ds}. The I_{leak} was 0.02μA at V_{ds} of 3.0V and RT, and was 2μA at V_{ds} of 5.0V and 85℃. These I_{leak} values are sufficiently low to allow the elimination of the drain bias switch. To our knowledge, the obtained leakage currents are the lowest values among reported enhancement-mode FETs [4,7,8]. Also, these are the almost same as that of HBT [9].

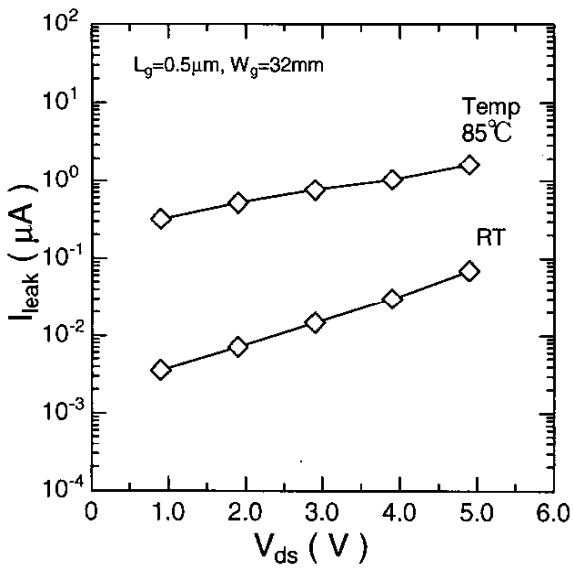

Fig. 6. V_{ds} and temperature dependence of I_{leak}

V. RF Power Performance

The 950MHz power performance of the 32mm W_g p^+-gate HJFET was evaluated at V_{ds} of 3.2V with a quiescent current (I_q) of 200mA. The optimum load and source impedances were determined through load-pull measurements. Fig. 7 shows the output power (P_{out}), power added efficiency (PAE) and associated gain (G_a) as a function of the input power (P_{in}). The p^+-gate HJFET exhibited a P_{out} of 35dBm, a PAE of 73% with a G_a of 11.9dB. Furthermore, the V_{ds} dependence of power performance was evaluated from 0.6V to 5.0V. Fig. 8 shows P_{out} and PAE as a function of V_{ds}. The device exhibited relatively flat PAE characteristics for V_{ds} of more than 1.0V. Even operated at V_{ds} of 1.0V, a high PAE of 70% with P_{out} of 0.35W was achieved. These excellent PAE characteristics are ascribed to the high I_{max} and low R_{on} for the developed p^+-gate HJFET.

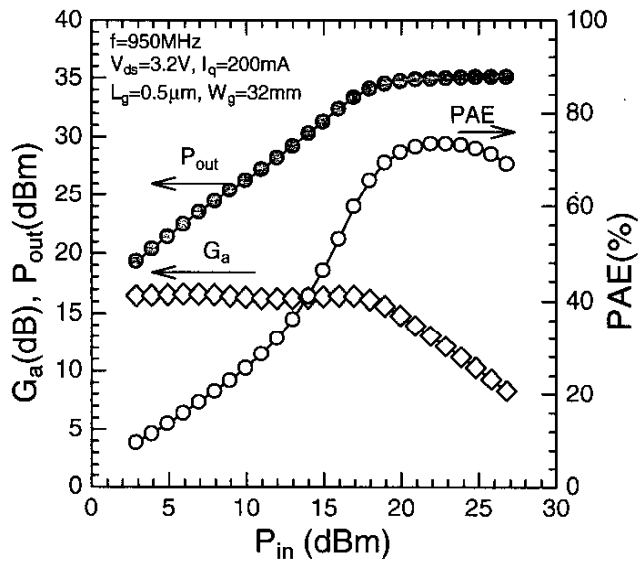

Fig. 7. P_{out}, PAE and G_a as a function of P_{in}

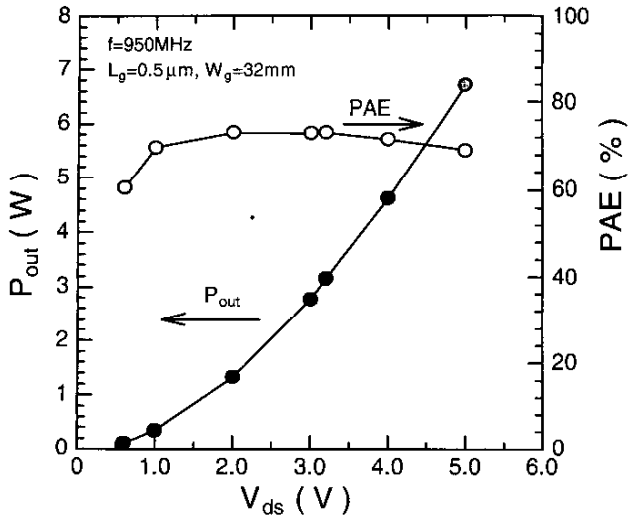

Fig. 8. V_{ds} dependence of P_{out} and PAE

VI. Conclusion

We have successfully developed enhancement-mode power HJFET utilizing selectively re-grown p^+-GaAs gate by MOCVD. The device has a high I_{max} of 400mA/mm with a high positive V_T of +0.5V. A small V_T standard deviation of 20mV was obtained. The device also exhibited the extremely low I_{leak}, which allows to eliminate the drain bias switch. Under single 3.2V operation, the 32mm p^+-gate HJFET exhibited a PAE of 73% with a P_{out} of 35dBm. Even operated at V_{ds} of 1.0V, a high PAE of 70% was achieved. These results indicate that the developed p^+-gate HJFET is a potential candidate for no drain bias switch and single voltage operation power amplifiers.

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